IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit comprising the steps of:

(1) fabricating at least one transistor in a silicon substrate;

(2) depositing a first dielectric layer on a top surface of said at least one transistor;

(3) depositing a metal catalyst layer on a top surface of said first dielectric layer;

(4) depositing a second dielectric layer on a top surface of said metal catalyst layer;

(5) etching at least one cavity through said second dielectric layer to the top surface of said metal catalyst layer, said at least one cavity being located above said at least one transistor;

(6) growing at least one carbon nanotube within said at least one cavity, said at least one carbon nanotube extending from the top surface of said metal catalyst layer to at least a top surface of said second dielectric layer; and,

(7) depositing a metallic, heat conducting layer on the top surface of said second dielectric layer, such that heat generated by said transistor is conducted from the top surface of said transistor to said metallic, heat conducting layer through said at least one carbon nanotube.

2. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein the first and second dielectric layers comprise silicon nitride.

3. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said metal catalyst layer comprises nickel.

4. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said metal catalyst layer comprises cobalt.

5. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said metallic, heat conducting layer comprises copper.

6. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said metallic, heat conducting layer comprises aluminum.

7. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said metallic, heat conducting layer is deposited within said at least one cavity in contact with said at least one carbon nanotube.

8. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein a top surface of said metallic, heat conducting layer is planarized following deposition, such that said at least on carbon nanotube does not extend above said top surface of said metallic, heat conducting layer.

9. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said at least one cavity is located above a drain of said at least one transistor.

10. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said at least one cavity is located above a source of said at least one transistor.

11. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit as recited in claim 1 wherein said at least one cavity is located above a heat generation area of said at least one transistor.

12. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die comprising the steps of:

(1) fabricating at least one transistor in a top surface of a silicon substrate;

(2) cutting at least one cavity within said silicon substrate, said at least one cavity extending through a back surface of said silicon substrate below said at least one transistor;

(3) depositing a catalyst layer within said at least one cavity; and,

(4) growing a plurality of carbon nanotubes within said at least one cavity, said plurality of carbon nanotubes extending from a bottom surface of said at least one cavity to the back surface of the silicon substrate.

13. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12, further comprising the step of:

(5) depositing a metallic, heat conducting layer on the back surface of said silicon substrate and within said at least one cavity, subsequent to the growth of said plurality of carbon nanotubes, said metallic, heat conducting layer in contact with said plurality of carbon nanotubes.

14. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 13, further comprising the step of:
(6) planarizing the back surface of said silicon substrate, such that said plurality of carbon nanotubes does not extend through said metallic, heat conducting layer.

15. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 13 wherein said metallic, heat conducting layer comprises copper.

16. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 13 wherein said metallic, heat conducting layer comprises aluminum.

17. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12 wherein said catalyst layer comprises nickel.

18. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12 wherein said catalyst layer comprises cobalt.

19. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12 wherein said at least one cavity is located below a drain of said at least one transistor.

20. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12 wherein said at least one cavity is located below a source of said at least one transistor.

21. (Withdrawn): A method for fabricating a heat conduction device in an integrated circuit die as recited in claim 12 wherein said at least one cavity is located below a heat generation area of said at least one transistor.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Previously presented): An integrated circuit die having enhanced power dissipation, comprising:

a substrate, having a top surface upon which power generating devices of said integrated circuit die are fabricated, said substrate having a backside surface essentially parallel to said top surface;

at least one cavity, extending from said backside surface a predetermined distance toward said top surface, said predetermined distance being less than the distance between said top surface and said backside surface; and

a heat conductive media contained within said at least one cavity, said media having a thermal conductivity greater than a bulk thermal conductivity of said substrate, such that heat produced by said power generating devices is transferred to the backside surface via said heat conductive media, wherein said heat conducting media comprises copper.

29. (Previously presented): An integrated circuit die having enhanced power dissipation, comprising:

a substrate, having a top surface upon which power generating devices of said integrated circuit die are fabricated, said substrate having a backside surface essentially parallel to said top surface;

at least one cavity, extending from said backside surface a predetermined distance toward said top surface, said predetermined distance being less than the distance between said top surface and said backside surface; and

a heat conductive media contained within said at least one cavity, said media having a thermal conductivity greater than a bulk thermal conductivity of said substrate, such that heat produced by said power generating devices is transferred to the backside surface via said heat conductive media, wherein said heat conducting media comprises carbon nanotubes.

30. (Previously presented): An integrated circuit die having enhanced power dissipation as recited in claim 29, wherein said at least one cavity is located directly below at least one power generating device in said substrate.

31. (Original): An integrated circuit die having enhanced power dissipation as recited in claim 30, wherein said at least one power generating device is a transistor having a drain, said at least one cavity being located directly below said drain.

32. (Original): An integrated circuit die having enhanced power dissipation as recited in claim 30, wherein said at least one power generating device is a transistor having a source, said at least one cavity being located directly below said source.